

### REMARKS

This amendment is submitted in response to the Examiner's Final Action dated April 16, 2004. Applicants have amended the independent claims herein by incorporating features of dependent claims (now canceled), which features more clearly and completely recite the novel features of the invention. No new matter has been added, and the amendments reduce issues for appeal and place the claims in better condition for allowance. Applicants respectfully request entry of the amendments to the claims. The arguments provided below reference the claims in their amended form.

### CLAIMS REJECTIONS UNDER 35 U.S.C. § 102

At paragraph 3 of the present Office Action, Claims 1-2, 5-6 and 9 are rejected under 35 U.S.C. § 102(e) as being taught by *Sproull* (U.S. Patent No. 6,038,646). *Sproull* does not anticipate Applicants' invention because *Sproull* does not teach each element recited within Applicants' amended claims.

Applicants' invention provides a method that enables an in-order processor to be operationally connected to a memory subsystem that completes memory access requests in a weakly consistent order. The method enables the processor-issued memory access request to be processed in any order at the memory subsystem but "completed" at the processor-level in the correct program order. This feature is made possible by a controller of the processor, which generates and places a barrier operation on the interconnect after each memory access request is issued (in-order) by the processor (*see* Figure 6C). While the memory access requests complete in any order (i.e., out-of-order) at the memory subsystem, they are forced by these associated barrier operations to return values to the processor in program order.

In one implementation, previously-issued barrier operations that are still pending are not considered an absolute bar to issuing additional memory access requests. A subsequent load request in the instruction sequence is "speculatively" issued with respect to the pending barrier operation. The data returned by that subsequent load request is, however, not allowed to be received by the processor until an acknowledgement is received for each/all previously-issued

barrier operation. This also enables all preceding operations in the instruction stream to complete (from a processor-perspective) in the order in which they were issued.

Applicants' claimed invention recites the following key components and associated functionality:

(1) "a controller associated with said processor that forwards said memory access requests to said memory system and which automatically places a barrier operation on said interconnect following each issuance of a memory access request to said memory system, wherein said barrier operation indicates a need to complete the data operations associated with the memory access requests in program order from the perspective of the processor, wherein said controller includes means for creating said barrier operations;" (Claim 1, emphases added) and

(2) "in response to receipt of said memory access instruction, generating a memory access request and a barrier operation; automatically initiating said barrier operation after said memory access request is issued to a memory system;" (Claim 9, emphases added).

Applicants' claimed invention thus requires every memory access operation be signaled as "complete" in the correct program order from the processor's perspective. Every memory access request is thus followed by a barrier operation. The controller actually generates these barrier operations following issuance of each memory access request.

Clearly, for a reference to anticipate Applicants' claimed invention, that reference must teach the above claim features. *Sproull* does not.

Examiner correctly recognizes that *Sproull* provides a memory interface (between a processor and memory subsystem) that is capable of multiple concurrent transactions or accesses (i.e., read and write operations and barrier operations) (Abstract). *Sproull* describes an instruction stream divided up into sets of instructions that are separated by a barrier operation. However, the barrier operations in *Sproull* are inserted (by a programmer) with the functional objective of separating successive memory operations when those successive operations reference the same memory address (*see*, col. 7, ll 60 – col. 9, ll 34). Thus, the *Sproull* barrier

operations are directed to programmer-specified memory protection based upon matching addresses, and not to the presently claimed controller-specified maintenance of instruction order from the perspective of the processor.

As is illustrated by the instruction stream of *Sproull's* Figure 3, a set of instructions may contain a series of memory access request that are issued by *Sproull's* processor without any barrier operation being placed after each issuance. In fact, the generation and placement of the MEMIBAR operations could not be an automatic function performed by a controller since it requires actual knowledge (known by the programmer) that a next/subsequent operation would access the same memory address. The instruction stream is thus provided with specific barrier operations at pre-programmed locations within the issuing sequence. Also, *Sproull* explains that the memory access instructions within a set may complete in any order with respect to each other (*id.*).

Thus, it is clear that *Sproull* does not teach "a controller... that ...automatically places a barrier operation on the interconnect following each issuance of a memory access request to said memory system." It is also clear that *Sproull* does not teach or contemplate actual generation of barrier operations whenever a memory access operation is encountered and issued to the interconnect.

The standard for a § 102 rejection requires that the reference teach each element recited in the claims set forth within the invention. As clearly outlined above, *Sproull* reference fails to meet this standard and therefore do not anticipate Applicants' invention.

#### **CLAIM REJECTIONS UNDER 35 U.S.C. § 103(a)**

At paragraph 10 of the present Office Action, Claims 3-4, 7-8 and 10-11 are rejected under 35 U.S.C. § 103(a), as being unpatentable over *Sproull* as applied to Claims 1, 5 and 9 above, in view of *Karp, et al.* (U.S. Patent No. 6,321,328). The above arguments, which overcome the 102 rejection of the independent claims also overcomes the 103 rejections of the present claims, which depend from the independent claims.

Atty. Docket No.: AT9-99-505  
Amendment B  
Page 7 of 9

Additionally, Applicants would reiterate the arguments proffered in Amendment A, with respect to the definition/meaning attributed to the term "speculative" within Applicants' claimed invention, versus the meaning of that term within *Karp*. As recited within the specification and claims, Applicants' invention provides the term speculative in the context of "ignoring" the status of a previously issued barrier operation and issuing a subsequent load request to the interconnect before the barrier operation completes.

*Karp*, in contrast, describes a conventional speculative issuance of an instruction, which depends on branch paths taken or not taken, etc. That is, *Karp* moves a load instruction up in the instruction sequence and the instruction is issued speculatively because "the compiler does not know if ... branch instructions will take a path away from the load instruction."

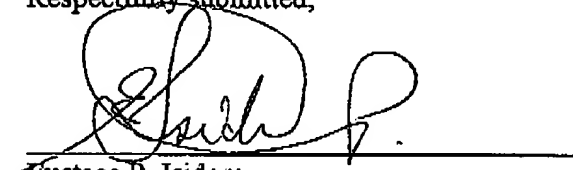
It is clear that *Karp's* use of that term is inherently different in functionality than what is recited by Applicants' claims. -It is also clear that *Karps'* use of that term is not suggestive of the specific functionality attributed to Applicants' speculative issuance of a load operation beyond a pending barrier operation. For these reasons, one skilled in the art would not find Applicants invention obvious in light of the combinations and the above claims are allowable.

**CONCLUSION**

Applicants have diligently responded to the present Office Action by amending the claims to more clearly recite the features unique to Applicants' invention in the independent claims. Applicants have further shown why the claims are not taught by or obvious over the cited references. The amendments and arguments overcome the §102 and §103 rejections, and Applicants, therefore, respectfully request reconsideration of the rejections and issuance of a Notice of Allowance for all claims now pending.

Applicants also request the Examiner contact the undersigned attorney of record at (512) 343-6116 if such would further or expedite the prosecution of the present Application.

Respectfully submitted,



Eustace P. Isidore

*Registered with Limited Recognition (see attached)*

Dillon & Yudell LLP

8911 North Capital of Texas Highway

Suite 2110

Austin, Texas 78759

512.343.6116

Atty. Docket No.: AT9-99-505

Amendment B

Page 9 of 9